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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/528,714	03/20/2000	Ryuichi Sunayama	826.1593/JDH	5805

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/528,714	SUNAYAMA ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2000 and 26 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-16 have been considered.

Specification

2. The disclosure is objected to because of the following informalities: Please correct the phrase "the address mode is sometimes changed while instruction is executed" on page 4, lines 14-15 to read --the address mode is sometimes changed while an instruction is executed--. Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Figure 1, element 2 on page 8, line 16. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5, 6, 8, 9, 10, 12, 13, 14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishikawa, U.S. Patent Number 5,142,630 (herein referred to as Ishikawa).

6. Referring to claim 1, Ishikawa has taught an instruction processing device, comprising:

a. A storage circuit storing address mode information of a fetched instruction with an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. A branch instruction control circuit controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction (Ishikawa column 2, lines 29-50).

c. A transfer circuit transferring the address mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed (Ishikawa column 4, lines 20-27 and Figure 1, element 11).

7. Referring to claim 2, Ishikawa has taught wherein said branch instruction control circuit stores address mode information of a branch destination of the branch instruction with an instruction address of the branch destination (Ishikawa column 1, lines 43-52).

8. Referring to claim 3, Ishikawa has taught wherein said branch instruction control circuit generates the address mode information of the branch destination based on the address mode information of the branch instruction (Ishikawa column 4, lines 44-59).

9. Referring to claim 5, Ishikawa has taught wherein said branch instruction control circuit outputs a signal indicating the address mode information and instruction address of the branch destination when issuing a branch destination instruction fetch request (Ishikawa column 4, lines 44-59).

10. Referring to claim 6, Ishikawa has taught wherein said branch instruction control circuit outputs a signal indicating whether the branch instruction is accompanied by an address mode change when control of the branch instruction is terminated (Ishikawa

column 4, lines 33-44). In regards to Ishikawa, it is inherent that there is a signal indicating an address mode change in order to load the address mode bit register.

11. Referring to claim 8, Ishikawa has taught the device further comprising:

a. A branch destination address generation circuit generating an instruction address of a branch destination of the branch instruction using the address mode information (Ishikawa column 2, lines 29-50).

b. Wherein said transfer circuit transfers the address mode information stored in the storage circuit to the branch destination address generation circuit when the branch instruction is executed (Ishikawa column 4, lines 20-27).

12. Referring to claim 9, Ishikawa has taught an instruction processing device, comprising:

a. A storage circuit storing mode information of a fetched instruction with an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. A branch instruction control circuit controlling a branch instruction using the mode information if the fetched instruction is the branch instruction (Ishikawa column 2, lines 29-50).

c. A transfer circuit transferring the mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed (Ishikawa column 4, lines 20-27).

13. Referring to claim 10, Ishikawa has taught an instruction processing device comprising:

a. A fetch circuit fetching an instruction (Ishikawa column 3, lines 23-25). In regards to Ishikawa, in order to fetch an instruction there must be a fetch circuit.

b. A storage circuit storing mode information of each fetched instruction as part of an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

c. A control circuit controlling an instruction process of each instruction based on the stored mode information (Ishikawa column 3, lines 25-35 and 43-65).

14. Referring to claim 12, Ishikawa has taught an instruction processing method comprising:

a. Handling mode information of an information processing apparatus, which is to be determined when fetching each instruction, as part of an instruction (Ishikawa column 1, lines 13-17).

b. Fetching an instruction (Ishikawa column 3, lines 23-25).

c. Storing mode information of the fetched instruction in each cycle of an instruction process of the fetched instruction (Ishikawa column 1, lines 43-52).

d. Controlling the instruction process for the fetched instruction based on the stored mode information (Ishikawa column 3, lines 25-35 and 43-64).

15. Referring to claim 13, Ishikawa has taught an instruction processing device comprising:

a. A storage means for storing address mode information of a fetched instruction with an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. Branch instruction control means for controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction (Ishikawa column 2, lines 29-5).

c. Transfer means for transferring the address mode information stored in the storage means to the branch instruction control means when the branch instruction is executed (Ishikawa column 4, lines 20-27).

16. Referring to claim 14, Ishikawa has taught an instruction processing device comprising:

a. A storage means for storing mode information of a fetched instruction with an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. Branch instruction control means for controlling a branch instruction using the mode information if the fetched instruction is the branch instruction (Ishikawa column 2, lines 29-5).

c. Transfer means for transferring the mode information stored in the storage means to the branch instruction control means when the branch instruction is executed (Ishikawa column 4, lines 20-27).

17. Referring to claim 15, Ishikawa has taught an instruction processing device comprising:

a. Fetching means for fetching an instruction (Ishikawa column 3, lines 23-25).

b. Storage means for storing mode information of each fetched instruction as a part of an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

c. Control means for controlling an instruction process of each instruction based on the stored mode information (Ishikawa column 3, lines 25-35 and 43-64).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa, U.S. Patent Number 5,142,630 (herein referred to as Ishikawa), as applied to claims 1 and 2 above, in view of Morisada, U.S. Patent Number 4,881,170 (herein referred to as Morisada).

20. Referring to claim 4, Ishikawa has not taught wherein said branch instruction control judges whether address mode information and an instruction address of a branch destination predicted by a branch prediction are correct using the address mode information and instruction address of the branch destination. Morisada has taught wherein said branch instruction control judges whether address mode information and an instruction address of a branch destination predicted by a branch prediction (Morisada

Abstract, lines 12-16) are correct using the address mode information and instruction address of the branch destination (Morisada column 3, lines 45-52). It would have been obvious to incorporate the prediction of Morisada, because it would prevent an access to memory in the wrong mode during prefetching, which would decrease execution time. Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the prediction of Morisada in the device of Ishikawa to decrease execution time of instructions.

21. Referring to claim 7, Ishikawa has not taught the device further comprising a branch history circuit relating address mode information and an instruction address of a branch instruction to address mode information and an instruction address of a branch destination, storing related address mode information and instruction addresses of the branch instruction and branch destination, and making a branch prediction for the fetched branch instruction. Morisada has taught a branch history circuit relating address mode information and an instruction address of a branch instruction to address mode information and an instruction address of a branch destination, storing related address mode information and instruction addresses of the branch instruction and branch destination, and making a branch prediction for the fetched branch instruction (Morisada Abstract, lines 4-16). It would have been obvious to a person of ordinary skill in the art to incorporate the branch history circuit of Morisada, because it would allow branch prediction, which increases the speed of a processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the branch history circuit of Morisada in the device of Ishikawa to increase processor speed.

22. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa, U.S. Patent Number 5,142,630 (herein referred to as Ishikawa) in view of Shiell et al., U.S. Patent Number 5,963,721 (herein referred to as Shiell).

23. Referring to claim 11, Ishikawa has taught an instruction processing device comprising:

a. A storage circuit storing mode information obtained when an instruction fetch request is issued with an instruction address for each port (Ishikawa column 1, lines 43-52 and column 3, lines 23-25).

b. A fetch circuit performing an instruction fetch based on mode information corresponding to a port to be used (Ishikawa column 4, lines 20-59).

24. Ishikawa has not taught the device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system. Shiell has taught a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system (Shiell column 1, lines 41-55; Figure 1; and Figure 2). In regards to Shiell, in order to examine the sequence of instructions, there must be multiple instruction fetch ports to fetch the instructions for examination. It would have been obvious to a person of ordinary skill in the art to incorporate the multiple fetch ports and out-of-order system, because this reduces the delay caused by stalls in the pipeline from branches. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiple fetch ports and out-of-order system of Shiell in the device of Ishikawa to minimize the effect of stalls in the pipeline.

25. Referring to claim 16, Ishikawa has taught an instruction processing device comprising:

a. Storage means for storing mode information obtained when an instruction fetch request is issued with an instruction address for each port (Ishikawa column 1, lines 43-52 and column 3, lines 23-25).

b. Fetch means for performing an instruction fetch based on mode information corresponding to a port to be used (Ishikawa column 4, lines 20-59).

26. Ishikawa has not taught the device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system. Shiell has taught a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system (Shiell column 1, lines 41-55; Figure 1; and Figure 2). In regards to Shiell, in order to examine the sequence of instructions, there must be multiple instruction fetch ports to fetch the instructions for examination. It would have been obvious to a person of ordinary skill in the art to incorporate the multiple fetch ports and out-of-order system, because this reduces the delay caused by stalls in the pipeline from branches. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiple fetch ports and out-of-order system of Shiell in the device of Ishikawa to minimize the effect of stalls in the pipeline.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also

show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Akihiro et al., Japanese Publication Number 04245334 A, contains a storage circuit and transfer circuit.

b. Masahiko, Japanese Publication number 61278935 A, contains a storage circuit and branch instruction control circuit.

c. Kuriyama et al., U.S. Patent Number 4,954,947, contains a storage circuit and branch control circuit.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

30. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

November 14, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100